# REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188



| 1. REPORT DATE *(DD-MM-YYYY)* | 2. REPORT TYPE | 3. DATES COVERED *(From – To)* |
|---|---|---|
| 13-02-2004 | Final Report | 26 October 2001 - 26-Jul-02 |

**4. TITLE AND SUBTITLE**

Memowire: Polycrystalline Silicon Memory Effects

**5a. CONTRACT NUMBER**
F61775-02-WD079

**5b. GRANT NUMBER**

**5c. PROGRAM ELEMENT NUMBER**

**6. AUTHOR(S)**

Dr. Adrain Ionescu

**5d. PROJECT NUMBER**

**5d. TASK NUMBER**

**5e. WORK UNIT NUMBER**

**7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)**

Swiss Federal Inst. of Tech. Lausanne
EPFL, DE-LEG
ELB Ecublens
Lausanne 1015
Switzerland

**8. PERFORMING ORGANIZATION REPORT NUMBER**

N/A

**9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)**

EOARD
PSC 802 BOX 14
FPO 09499-0014

**10. SPONSOR/MONITOR'S ACRONYM(S)**

**11. SPONSOR/MONITOR'S REPORT NUMBER(S)**
SPC 01-4079

**12. DISTRIBUTION/AVAILABILITY STATEMENT**

Approved for public release; distribution is unlimited.

**13. SUPPLEMENTARY NOTES**

**14. ABSTRACT**

This report results from a contract tasking Swiss Federal Inst. of Tech. Lausanne as follows: The contractor will study and report on materials and device information for the polysilicon memory project. Contractor to provide materials information on how polysilicon, silicon dioxide, and the polysilicon/silicon dioxide interfaces behave under temperature and electric field stresses. Specific device information to be applicable to e-beam fabricated memory devices, the specific effect under study is the nature and origin of the hysteresis effect.

**15. SUBJECT TERMS**
EOARD, Electronic Devices, Materials, Memory, silicon

| 16. SECURITY CLASSIFICATION OF: | | | 17. LIMITATION OF ABSTRACT | 18, NUMBER OF PAGES | 19a. NAME OF RESPONSIBLE PERSON |
|---|---|---|---|---|---|
| a. REPORT | b. ABSTRACT | c. THIS PAGE | | | CARL A. KUTSCHE, Lt Col, USAF |
| UNCLAS | UNCLAS | UNCLAS | UL | | 19b. TELEPHONE NUMBER *(Include area code)* +44 (0)20 7514 4505 |

# MEMOWIRE – 2nd progress report

Edited by Serge Ecoffey

Date: December 23rd, 2002

**Participants:**
S. Ecoffey, PhD candidate, D. Bouvet, PhD
A.M. Ionescu, Professor
Electronics Labs, Institute of Microelectronics and Microsystems
Swiss Federal Institute of Technology Lausanne, Switzerland

## 1. Introduction and update

According to the EOARD project: "Memowire: Polycrystalline Silicon Memory Effects" and the "Memowire: 1st progress report", this report provides some first information about the electrical properties of an ultra-thin (10nm) ion implanted polysilicon film. Thin polysilicon films have been implanted with Boron and Phosphorous with energies of 5 and 25 keV and doses tuned by 2D-numerical simulations with ATHENA in order to achieve a target of $5x10^{17}$ dopants/cm$^3$. The electrical characterization has been carried out by using some dedicated test structures: Van der Pauw structures, 2 and 4 contacts resistivity lines, capacitances and 4 contacts Kelvin structures.
The **first section** of the report corresponds to the **technical description of the thin film**, the ion implantation parameters and the 4 contacts Kelvin test structures used for the polysilicon to polysilicon contacts characterization. The **second section**, gives an overview on the **electrical characterization** and **SIMS measurements results**, first for the ultra-thin polysilicon film and then for the 4 contacts Kelvin measurements. Note that all these investigations have been conducted on large structures and have been considered as mandatory before fabricating the narrow wires on ultra-thin polysilicon.

We can claim that these results highlighted some key potential problems to be solved and, even if the final e-beam fabrication of the nanowires has been delayed, we are able now to provide an improved technological flow (reported in the final sub-chapter) for the final realization. It is worth noting that we have detected a new potential problem associated with a low temperature budget of polysilicon annealing (highly needed to keep the grain size less than 10 nm): the ***limited activation of the dopants*** that could substantially increase the wire resistance and modify their conducting behaviour; this problem is proposed to be solved by a special implant into hot substrate.

After a meeting on December 6th 2002, with technological staff of LETI we have planned the **e-beam work on LETI platform in March 2003** and the **electrical test of the nanowires in April-May 2003**, which is the most realistic dead-line to end up the first part of the MEMOWIRE project.

In terms of technological splits, 25 wafers have been sent for implantation to IBS*. Five of them were used for polysilicon to polysilicon contact measurement and were phosphorous doped at 25keV. The remaining twenty wafers have been used for the polysilicon ultra-thin film characterization with different implant conditions: (i) boron doping at 10keV (5 wafers), (ii) boron doping at 25 keV (5 wafers), (iii) phosphorous doping at 10keV (5 wafers), and (iv) phosphorous doping at 25 keV (5wafers). All wafers have then been sent back to IBS* for the activation anneal at 800°C for times varying from 150s to 270s. After that, five wafers have been sent for a SIMS profile characterization at EVANS Technologies** and the residual wafers have been processed at EPFL for the test structures realisation (process flow described on *Appendix3.1*) and the electrical measurements.

# 2. Technical description

## 2.1. LPCVD deposition of the ultra-thin polysilicon thin film

The ultra-thin polysilicon fi[1]lm has been deposited in a standard horizontal LPCVD furnace using silane as a gas source. A two-step process has been chosen: the **first step consists of an amorphous phase deposition at 500°C**, whereas **the second step is the thin film crystallisation at 800°C after implantation**.

The film has been deposited on a p-type <100> oriented 4 inch silicon substrate. A **7nm underlying dry oxide has been grown as a pseudo-gate oxide**. To control the ion implantation, a sputtered oxide cap with various thickness (from 20nm to 80nm) has been deposited on the polysilicon film.

## 2.2. Ion implantation: simulation and implant parameters

Due to the unusually thin thickness of the polysilicon film, simulations have been run to determine the appropriate **(i) energy, (ii) dose and (iii) thickness of the cap oxide layer** for a $5 \cdot 10^{17} cm^{-3}$ final concentration. The simulations have been carried out using ATHENA, a 2D process simulation software from Silvaco International. A SIMS Verified Dual Pearson (SDVP) model has been exploited.

After the ion implantation simulation based study (cf. "Memowire: 1st progress report"), we have chosen **two doping species that are $BF_2$ and P with two different energies of implantation: 10 and 25 keV.**

The polysilicon film thickness has been maintained at 10nm and the final dose has been fixed at $5 \cdot 10^{17}$ $cm^{-3}$. The *Table I* summarizes the four final splits of implantation in terms of: (1) doping species, (2) initial implant dose, (3) energy implant, (4) screen oxide thickness, and (5) temperature and (6) duration of annealing.

| Dopant | Dose [$cm^{-2}$] | Energy [keV] | Oxide [nm] | Temp. [°C] | Time [s] |
|---|---|---|---|---|---|
| B | $2\ 10^{13}$ | 10 | 19 | 800 | 180 |
| B | $3\ 10^{14}$ | 25 | 49 | 800 | 180 |
| P | $1.3\ 10^{14}$ | 10 | 37 | 800 | 180 |
| P | $3\ 10^{14}$ | 25 | 80 | 800 | 180 |

***Table I*:** optimised characteristics for a 10nm polysilicon film implantation.

* Ion Beam Services (IBS), ZI Peynier-Rousset, 13790 Peynier, France.
** Cascade Scientific Ltd/Evans Europa, Uxbridge, Middlesex UB8 3PH, U.K.

### 2.3. Four contacts Kelvin structures: process and structure description

The 4 contacts Kelvin structures have been exploited to determine the resistivity of a contact between two polysilicon layers. The first polysilicon film, deposited on top of the gate oxide, acts as a barrier when contacting the ultra-thin polysilicon (see Appendix: *Appendix1.1*). Thus in case of metal diffusion through the 10nm polysilicon, the underlying gate or tunnel oxide is protected by this 0.25µm polysilicon.
The **first polysilicon film has been deposited by LPCVD at 640°C and then $POCl_3$ doped at 880°C**. The **second polysilicon layer deposited on top of the first, is the ultra-thin film as described before**.

The use of a 4 contacts Kelvin structure (see *Appendix1.2*) allows determining the value of the contact resistivity itself without the problem of the arms resistance.

No etching is possible to remove the native oxide on the first polysilicon layer before the deposition of the ultra-thin film. Therefore, the two polysilicon layers stack is ion implanted to reduce or cancel the effect of this insulating film. The implantation parameters have been chosen after simulation with ATHENA, as used before. The doping specie is **Phosphorous, with a doping energy of 25keV and an initial dose of $10^{13}$ $cm^{-2}$**. After implantation, **the films are annealed at 800°C for 180s**.

## 3. Electrical results

### 3.1. Ultra-thin polysilicon film resistivity

In order to evaluate the resistivity of the ultra-thin polysilicon film different type of structures with varying geometries and dimensions have been designed: **Van der Pauw** (VdP) structures (circles, squares and crosses), **cross bridge structures**, **square resistors**, **4-contact lines**, **4-contact serpentines** and **4-contact Kelvin resistor** without the underlying polysilicon barrier.

The measurements have been carried out with a low current (~10 fA) CASCADE micro-prober and a HP 4156C analyser from Agilent Technologies.

All the plots and results associated to the electrical measurements are not given in the text. They are distributed between the ***Appendix 1*** for the essential measurements, and the ***Appendix 2*** for the secondary measurements.

The resistivity measurements results suggest that the gate oxide has lost its insulating properties due to metal diffusion through the polysilicon film or too high-energy implantation. On the ***Appendix 1.3*** we can see two pseudo-capacitance plots. Those plots have been obtained by applying a potential Vs on (a) a 500µmx500µm ultra-thin polysilicon square and (b) on the frontside of the wafer. The associated current on the backside of the substrate Ig (Vg = 0) and on the probe Is are then quantified. It is clearly shown that all the current that is extracted from the probe flows in the substrate through the 7nm gate oxide (Ig always equals Is). Increasing the voltage increases the leakage in the substrate. Furthermore, the current measured is lower when connecting the polysilicon and/or less big squares (see ***Appendix 2.1*** **to** ***2.3***).

This leakage explains the lack of coherence between the different VdP or other resistivity measurements. As an example, we can see on the ***Appendix 1.4*** the plot derived from a round VdP structure of $10^6 \mu m^2$. A variable voltage Vg has been applied on probe 1 and the consecutive current has been measured on probe 1 (Is) and 3 (Id). A voltage is then measured between the probes 2 and 4 and by dividing this potential by the current on one of the probe (if both current are equal), we obtain the sheet resistance. It can be clearly seen on the plot, that the sheet resistance is not constant at all, and moreover is spread out on 7 decades. Also, Is and Id are not always equal, what confirms leakage to the substrate.

The same measurements have been performed on various kinds of VdP structures and on 4 contact Kelvin structures without the underlying 0.25µm doped polysilicon. The results are given on the ***Appendix 2.4* to *2.9***. They show the same lack of coherence than the round VdP structures described above.

There are two ways to explain the origin of this leakage: (i) **AlSi diffusion through the 10nm of polysilicon and the 7nm of oxide** (direct connection to the substrate); (ii) **too high implantation dose or energy**: the dopants have diffused in the oxide layer, diminishing the insulating properties of this one.

The **SIMS profile obtained from the implantations seems to show that the second proposition is the most adequate**. Indeed, if we look at the SIMS profile given on the ***Appendix 1.5*** (see also ***Appendix 2.10* to *2.12***) we can see that the concentration of boron in the gate oxide varies from $10^{17}$ to $3\cdot10^{18}cm^{-3}$. Furthermore, the polysilicon effective doping concentration is set around $3.5\cdot10^{18}cm^{-3}$ even though the simulation has located it at $5\cdot10^{17}cm^{-3}$. However, other **private communication with ion implantation experts support more the first explanantion**. Indeed the annealing step at 800°C during 180s should be able to activate only 5 to 10% of the dopants, which makes the second proposition inadequate.

Nevertheless more tests are now planned to understand more the origin of this leakage. Test structures with a thicker gate oxide, and/or with a polysilicon pad under the contact areas will be processed with the same implantation conditions but a higher annealing temperatures. On the other hand, this is not a solution for the implanted nanowires because the grain sizes will increase much more.

Another manner to determine whether the leakage comes from a too high energy/dose implantation or a metal diffusion to the substrate is under investigation: **hot implantation**. This particular process allows to use lower annealing temperatures for the dopants activation and so to control the grain sizes. It is the final technological solution envisioned for this project.

### 3.2. Four contacts Kelvin resistor measurements

The 4 contacts Kelvin measurements are executed by forcing a current $I_{13}$ through the probes 1 and 3 (see *Appendix 3*) and by measuring the differential voltage $V_{24}$ between the probes 2 and 4. The contact resistance $R_c$ is

$$R_c = \frac{V_{24}}{I_{13}} \qquad (1)$$

which is simply the ratio of the voltage to the current. The specific contact resistivity $\rho_c$ is calculated from $R_c$ through the relation

$$\rho_c = R_c A_c \qquad (2)$$

where $A_c$ is the contact area.

Note that thanks to the underlying polysilicon, the gate oxide has conserved its insulating properties, so **these structures were functionally successful compared to the previous ones**.The *Appendix 1.6* presents a quasi-static C-V measurement (QSCV) on a 500µmx500µm polysilicon square. This QSCV has been performed with the same HP 4156C mentioned above. We can see that **the value of the capacitance measured is consistent with the theoretical value of 1.5nF (7nm dry oxide), which confirms the fully functionality of the designed structure.**Other results performed on comb and circle capacitances (see *Appendix 2.13* and *2.14*) confirm this observation.

**Remark:** It has to be specified that before all the effective contact resistance measurements a current ramp has been applied on the device (between probes 1 and 3) in order to breakdown the oxide that has grown on the first polysilcon layer down. The plot of the *Appendix 1.7* shows

that a minimum current of 1µA is necessary to breakdown this native oxide. This native oxide should be eliminated in the final integration.

The *Appendix 1.8* corresponds to a Kelvin resistor measurement of a 10x10µm contact. The current $I_{13}$ is given on the X-axis and the associated voltage $V_{24}$ and contact resistance $R_c$ are reproduced on the Y-axis. We can see that $R_c$ reaches a plateau between 10nA and 1µA and then decreases with an increasing current. The **value of the plateau is about 20kOhm** while it decreases to 300Ohm at 10mA. This behaviour can **very probably be related to the self-heating of the contact at high current densities (resulting in a decrease of polysilicon resistivity).** The high resistance value is explained by the lack of dopant activation due to the low temperature used for annealing.
If we report the value of $R_c$ measured for the plateau versus the contact area we obtain the plot given in *Appendix 1.9*. This plot is derived from the measurements done on contacts of 2, 3, 5 and 10µm (see *Appendix 2.15* to *2.17*). It seems that when the contact size increases, the contact resistance decreases. This behaviour is consistent, but a plot the specific contact resistivity $\rho_c$ versus the contact area $A_c$ (see *Appendix 1.10)* shows that $\rho_c$ increases with $A_c$: the self heating due to contact size combined with the lack of activation can explain this behaviour.

The plots on *Appendix 1.11, 2.18* and *2.19* show resistivity measurements performed on serpentines with 5, 11 and 111 lines (100µm x 10µm). A 5 lines serpentine is described on the *Appendix 1.11*. A current $I_{14}$ is forced between probe 1 and 4 and the differential voltage associated $V_{23}$ is sensed between probes 2 and 3. We can see that the resistances associated with those structures spreads out from 3kOhm for a 5 lines serpentine to 80kOhm for a 111 lines serpentine what confirms the lack of dopant activation.

## 4. Project continuation

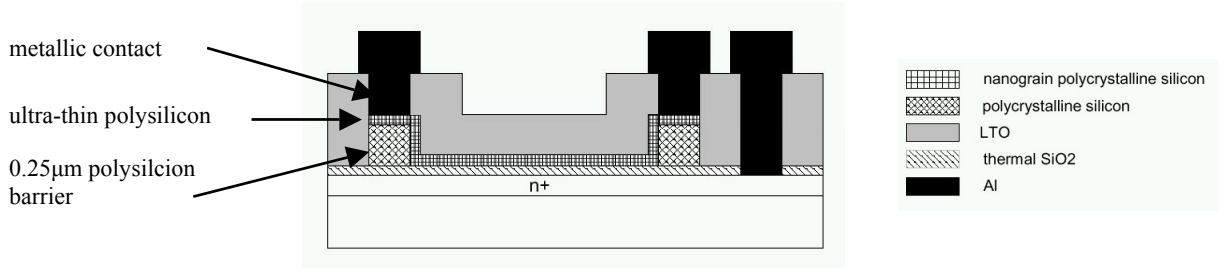
The need to **combine less than 10nm polysilicon grain sizes with ion implantation annealing has lead us to underestimate the temperature and time of annealing for dopant activation**. Thus the polysilicon films appear to be much highly resistive than expected and the Kelvin structures have shown high resistance contact properties. This resistance decreases with the current, due to self-heating.

Furthermore, **we have emphasized the how critical is the problem of taking a contact on a 10nm polysilicon film deposited on a 7nm dry oxide**. A diffusion of the metal through the polysilicon and the oxide and/or a too high dopant concentration in the oxide can explain the high leakage to the substrate that we experimentally observed.

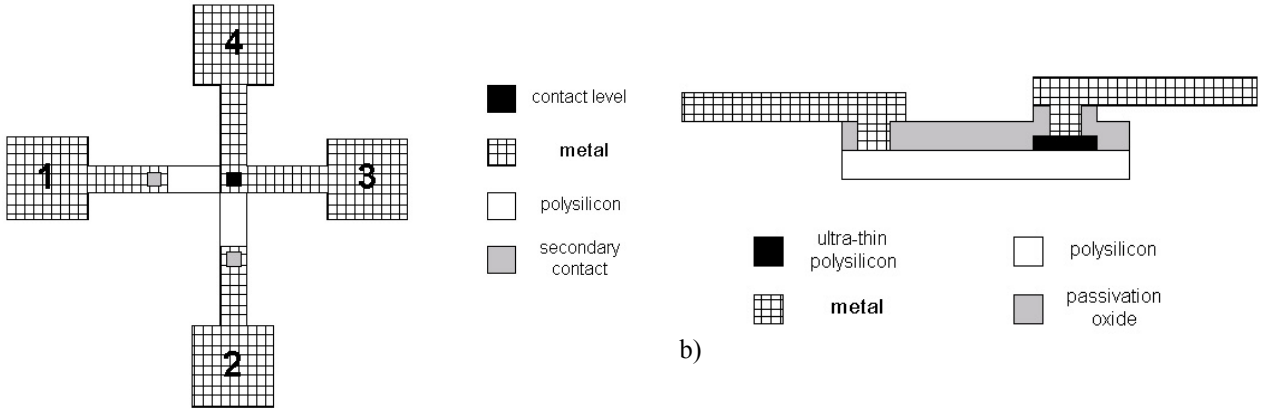
We can also conclude that the 2D numerical simulations with ATHENA can only gives order of magnitude of the equivalent doping in ultra-thin films and SIMS investigation and experimental calibration is absolutely needed.

These remarks have driven a **modification of the ion implantation process (see *Appendix 3.1*).** Two alternatives have been chosen: (i) a **hot implantation** and/or (ii) an **in-situ doped polysilicon deposition**. The first alternative allows to lower or even cancel the annealing step because the implantation takes place at 500°C (60% activation) or 600°C (80% to 100% activation). However, **temperature dependent simulation should be performed using a Monte Carlo instead of the SVDP model** (our group at EPFL dedicated early December a special fund to this needed licence under ATHENA software). We are planning to have electrical measurements for this alternative around mid-April, if no unexpected problem arises. The second alternative simply eliminates the implantation and annealing steps. Though **it needs modification of the LPCVD reactor (gas lines should be brought to the tube) and a study of the deposition parameters (gas pressure, temperature, gas mixes proportion)**. The modification of the furnace will take few months, so via this solution the delay for the final nanowires would be longer (end of June in the best case). We have decided to concentrate our efforts on the first solution as more realistic for the project dead-lines.

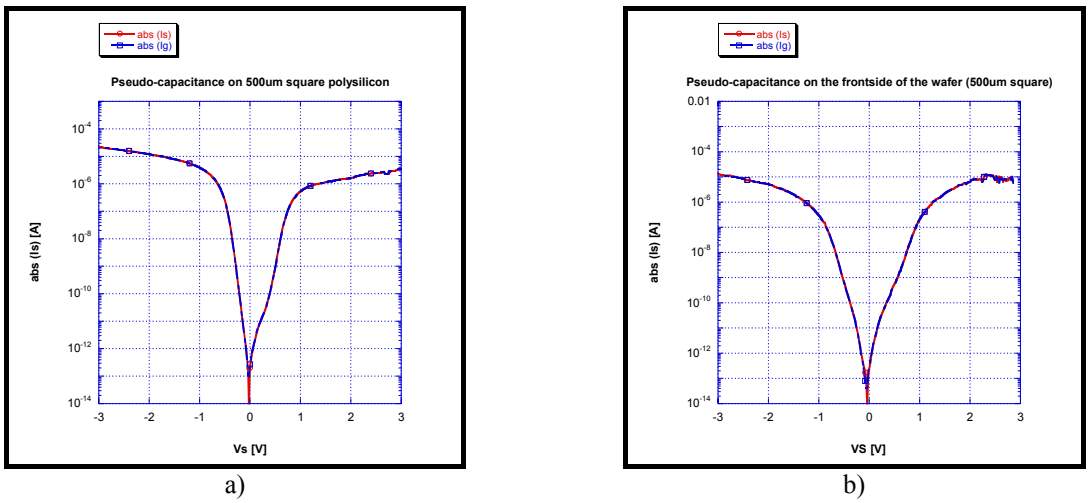
# APPENDIX 1



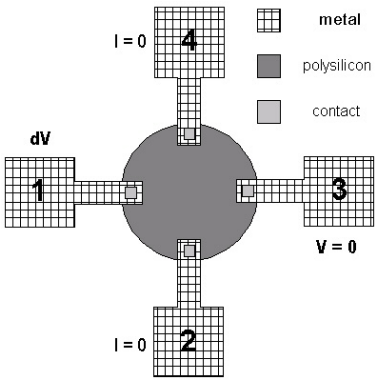

*Appendix 1.1*: cross-section view of the polysilicon to polysilicon contact region.



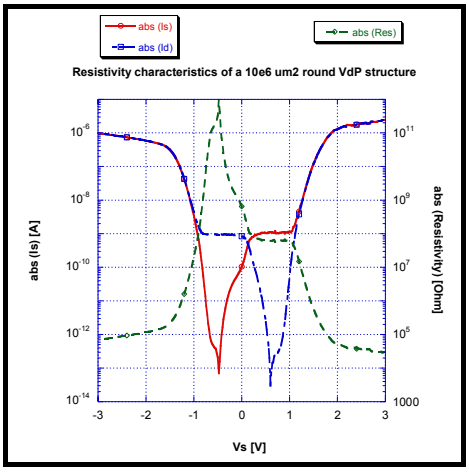

*Appendix 1.2*: schematic representation of the 4 contacts Kelvin structure: a) plan view; b) cross section.




*Appendix 1.3*: pseudo capacitance measurements on a 500µm by 500µm ultra-thin polysilicon square: contact on top of a) the polysilicon layer; b) the substrate.

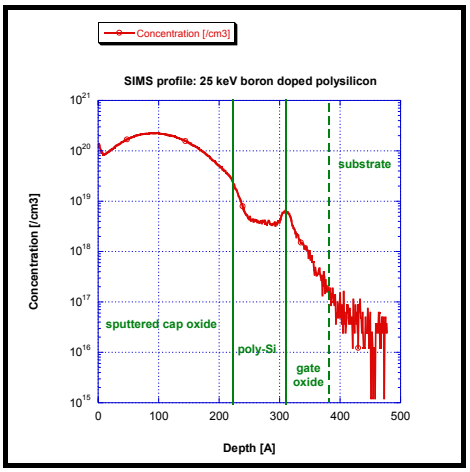



a)

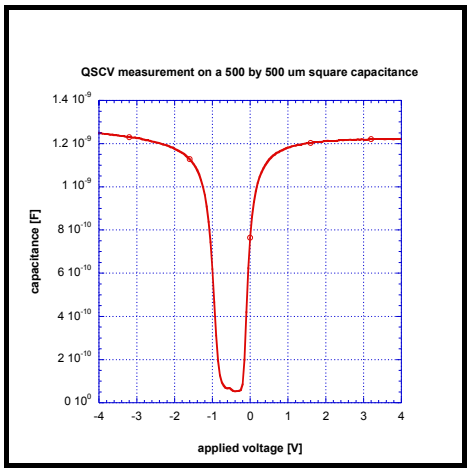



b)

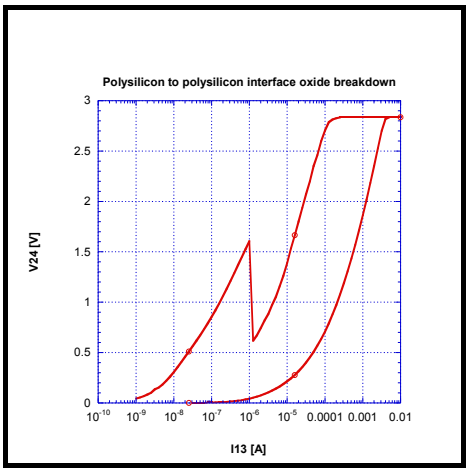
*Appendix 1.4*: $10^6$ µm$^2$ round VdP structure: a) schematic representation; b) electrical characteristics associated.



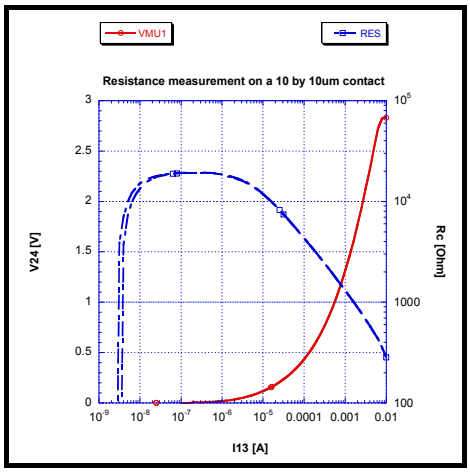

*Appendix 1.5*: SIMS profile of a 25 keV boron doped ultra-thin (10nm) polysilicon film.



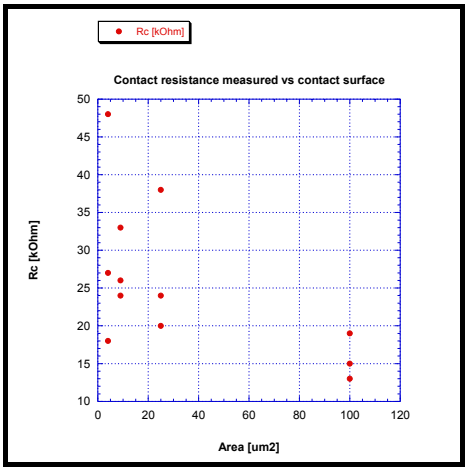

*Appendix 1.6*: QSCV measurement on a 500 by 500µm polysilicon square on 7nm oxide.



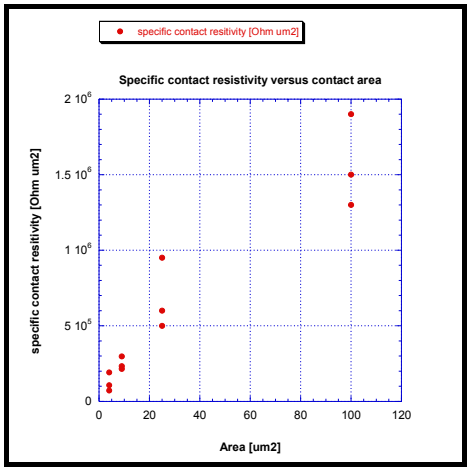

*Appendix 1.7*: interface native oxide breakdown.




*Appendix 1.8*: resistance measurements of: a 10 by 10µm polysilicon to polysilicon contact.

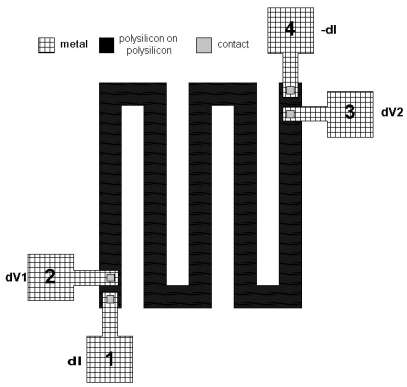


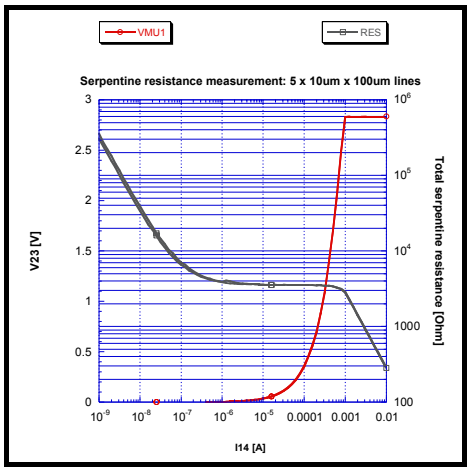

*Appendix 1.9*: contact resistance measured $R_c$ versus contact area $A_c$.




*Appendix 1.10*: specific contact resistivity $\rho_c$ versus contact area $A_c$.

a)

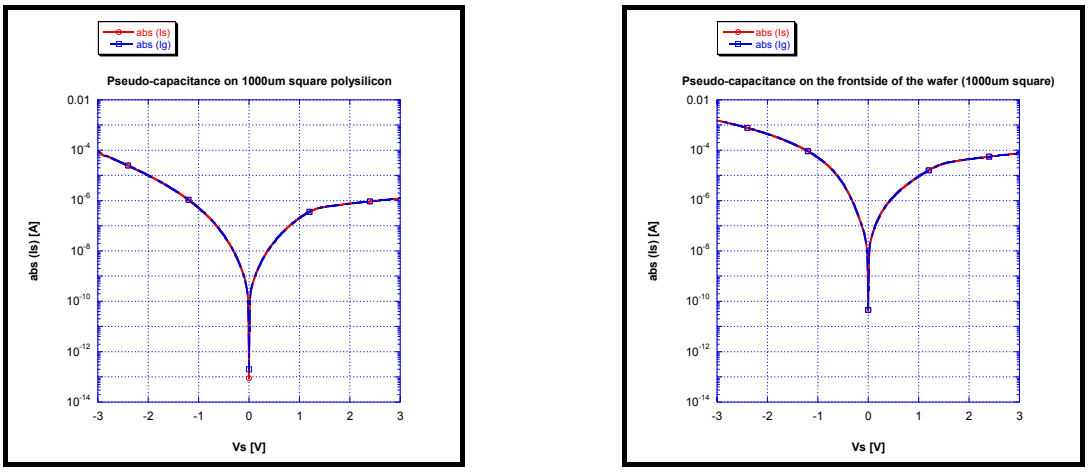



b)

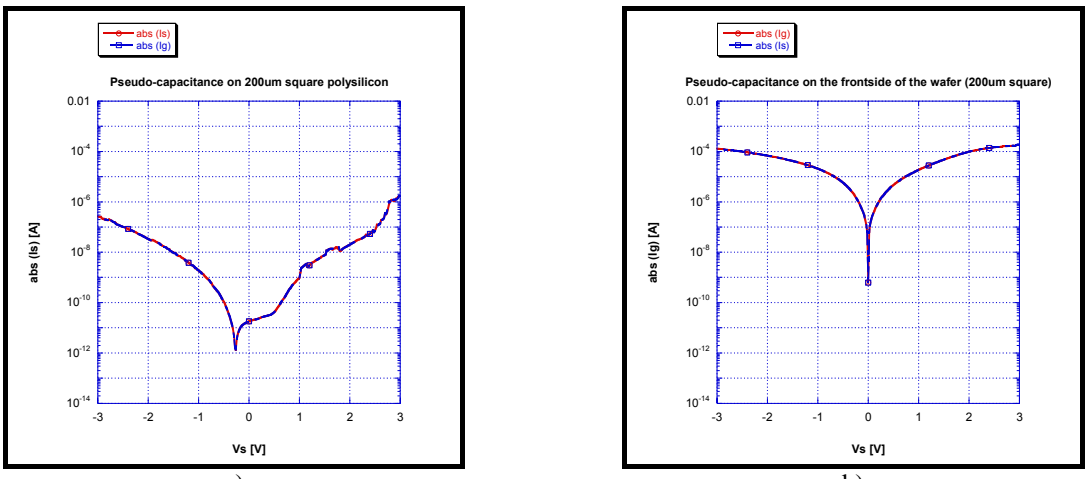
*Appendix 1.11*: 5 lines (10µm x 100µm) serpentine structure: a) schematic representation; b) electrical characteristics associated.

# APPENDIX 2



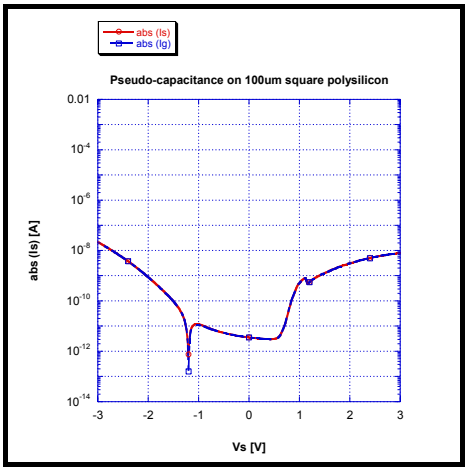

a) b)

*Appendix 2.1*: pseudo capacitance measurements on a 1000µm by 1000µm ultra-thin polysilicon square: contact on top of a) the polysilicon layer; b) the substrate.

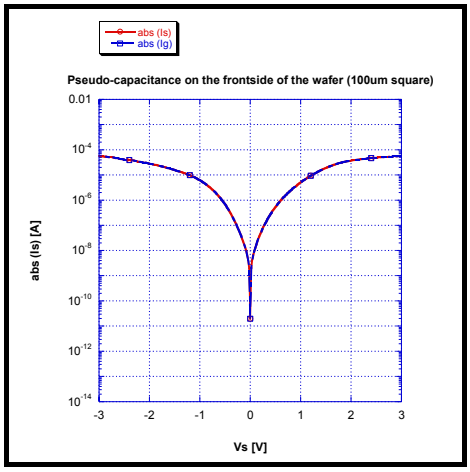



a) b)

*Appendix 2.2*: pseudo capacitance measurements on a 200µm by 200µm ultra-thin polysilicon square: contact on top of a) the polysilicon layer; b) the substrate.

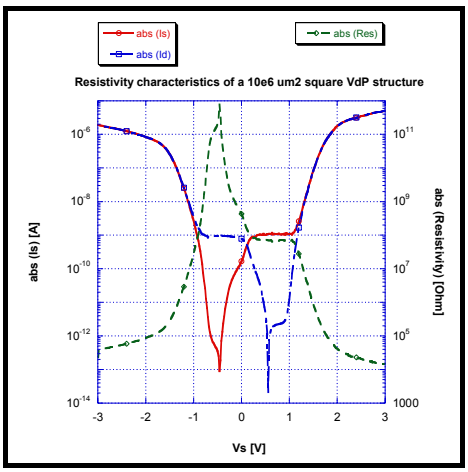



a)

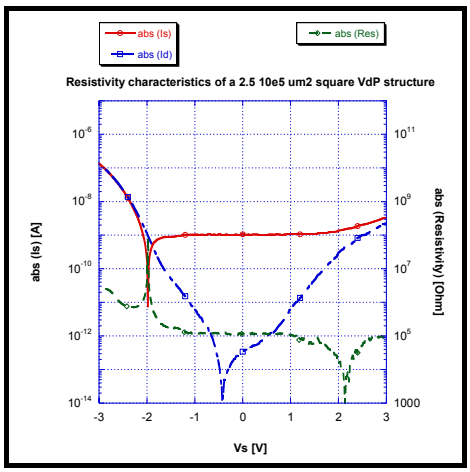



b)

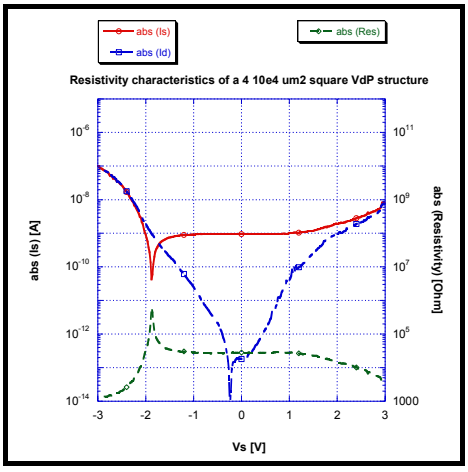
*Appendix 2.3*: pseudo capacitance measurements on a 100µm by 100µm ultra-thin polysilicon square: contact on top of a) the polysilicon layer; b) the substrate.



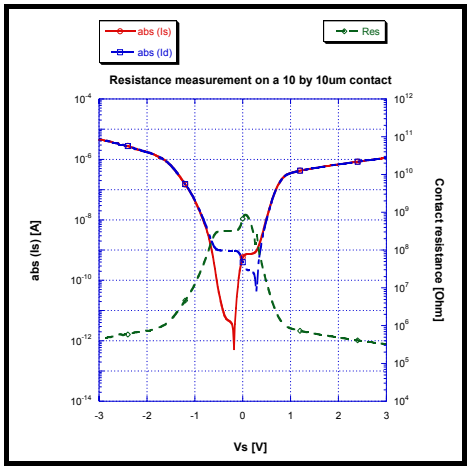

*Appendix 2.4*: electrical characterisitics of a $10^6$ µm$^2$ polysilicon square VdP structure.



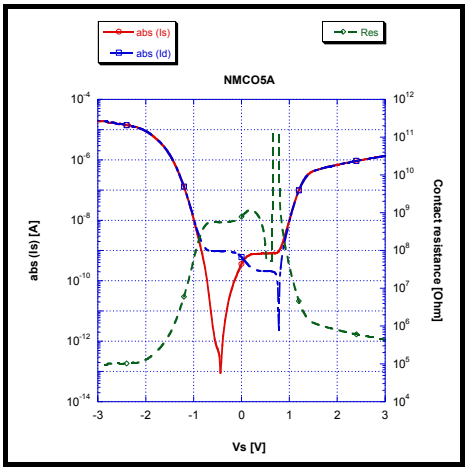

*Appendix 2.5*: electrical characterisitics of a 2.5 $10^5$ µm$^2$ polysilicon square VdP structure.



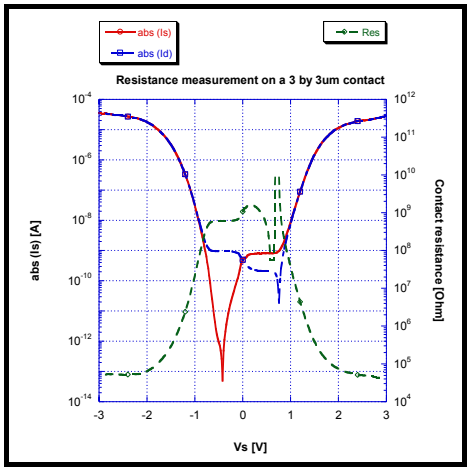

*Appendix 2.6*: electrical characterisitics of a 4 $10^4$ µm$^2$ polysilicon square VdP structure.



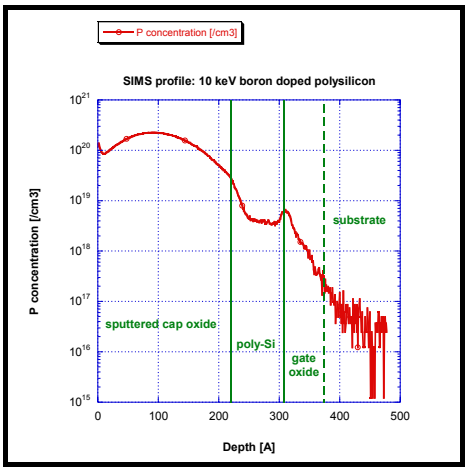

*Appendix 2.7*: resistance measurements of a 10 by 10µm metal on ultra-thin polysilicon contact.



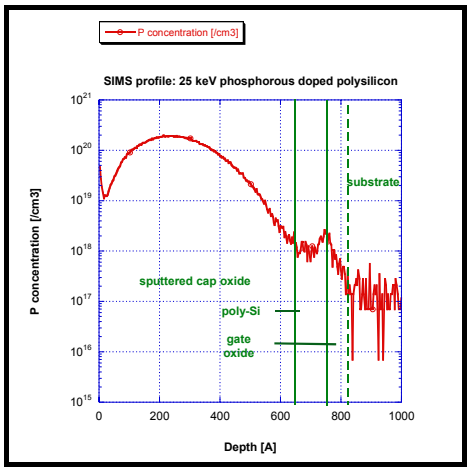

*Appendix 2.8*: resistance measurements of a 5 by 5µm metal on ultra-thin polysilicon contact.



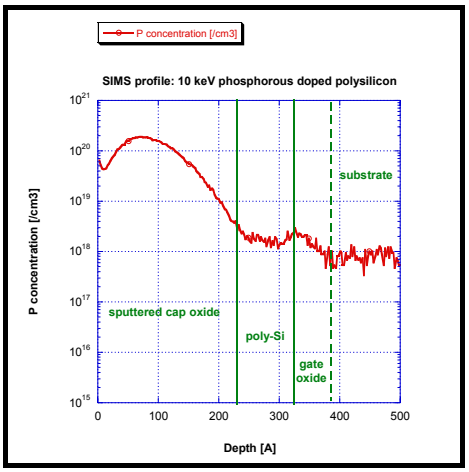

*Appendix 2.9*: resistance measurements of a 3 by 3µm metal on ultra-thin polysilicon contact.



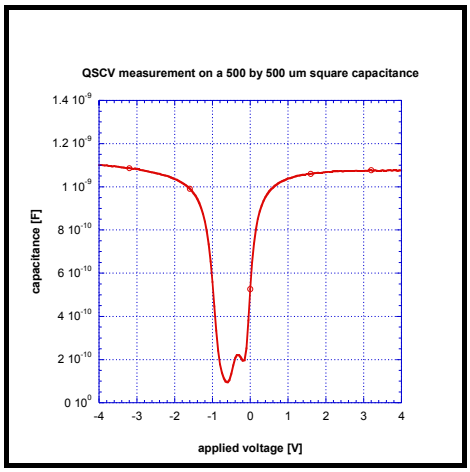

*Appendix 2.10*: SIMS profile of a 10 keV boron doped ultra-thin (10nm) polysilicon film.



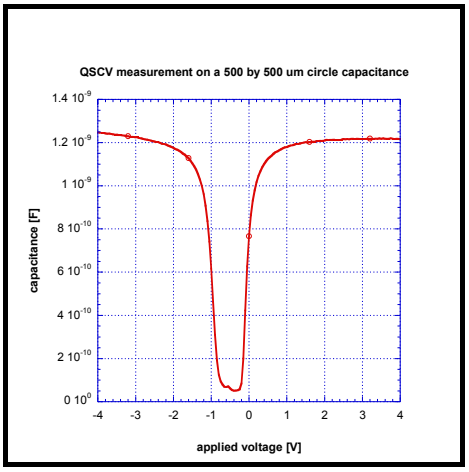

*Appendix 2.11*: SIMS profile of a 25 keV phosphorous doped ultra-thin (10nm) polysilicon film.



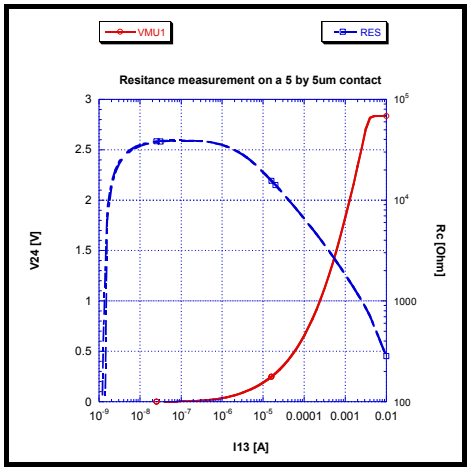

*Appendix 2.12*: SIMS profile of a 10 keV boron doped ultra-thin (10nm) polysilicon film.



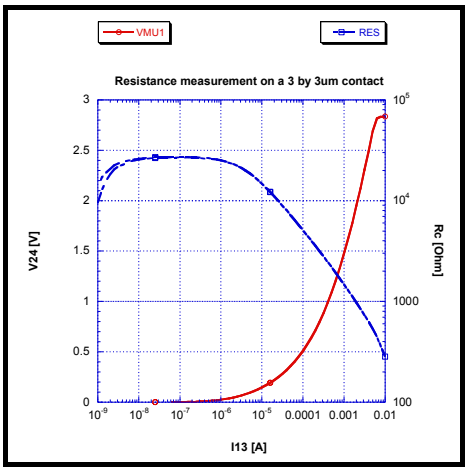

*Appendix 2.13*: QSCV measurement on a 500 by 500µm polysilicon comb on 7nm oxide.



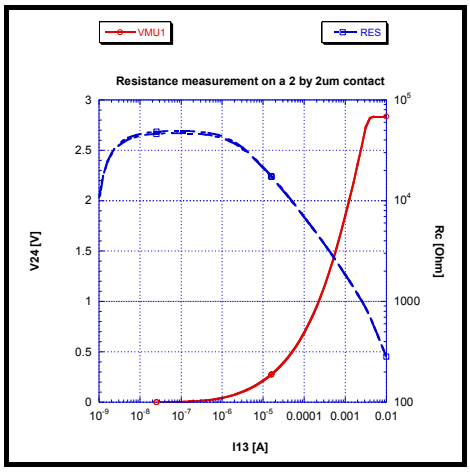

*Appendix 2.14*: QSCV measurement on a 500 by 500µm polysilicon circle on 7nm oxide.



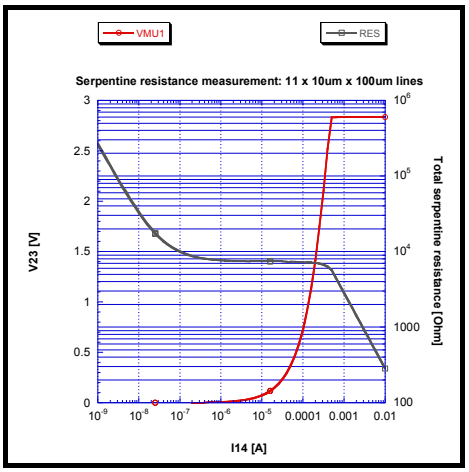

*Appendix 2.15*: resistance measurements of: a 5 by 5µm polysilicon to polysilicon contact.



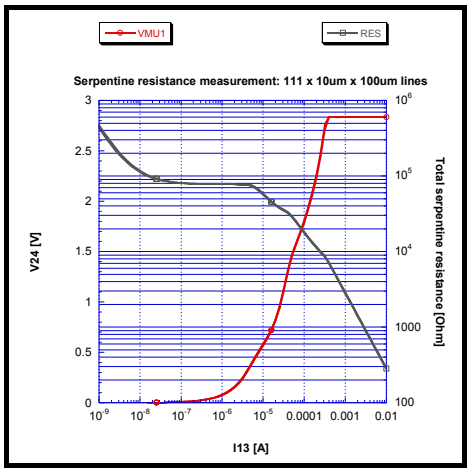

*Appendix 2.16*: resistance measurements of: a 3 by 3µm polysilicon to polysilicon contact.




*Appendix 2.17*: resistance measurements of: a 2 by 2µm polysilicon to polysilicon contact.




*Appendix 2.18*: electrical characteristics of a 11 lines (10µm x 100µm) serpentine structure.




*Appendix 2.19*: electrical characteristics of a 111 lines (10µm x 100µm) serpentine structure.

# APPENDIX 3

| Steps | Actual Process | Hot Implantation Process | In-situ doped process |
|---|---|---|---|
| 1 | Dry oxidation (7nm) | Dry oxidation (7nm) | Dry oxidation (7nm) |
| 2 | Underlying poly-Si deposition (0.25um) | Underlying poly-Si deposition (0.25um) | Underlying poly-Si deposition (0.25um) |
| 3 | POCl3 doping | POCl3 doping | POCl3 doping |
| 4 | Underlying poly-Si etching | Underlying poly-Si etching | Underlying poly-Si etching |
| 5 | Ultra-thin poly-Si deposition | Ultra-thin poly-Si deposition | Ultra-thin poly-Si deposition |
| 6 | Ultra-thin poly-Si etching | Ultra-thin poly-Si etching | Ultra-thin poly-Si etching |
| 7 | LTO cap oxide deposition | LTO cap oxide deposition | LTO cap oxide deposition |
| 8 | Standard ion implantation | **Hot ion implantation** | **No implantation** |
| 9 | Dopant activation anneal | **No or low temperature and time anneal** | **No anneal** |
| 10 | LTO passivation oxide deposition | LTO passivation oxide deposition | LTO passivation oxide deposition |
| 11 | Contact opening | Contact opening | Contact opening |
| 12 | Contact standard implantation | **Hot ion implantation** | **No implantation** |
| 13 | Dopant activation anneal | **No or low temperature and time anneal** | **No anneal** |
| 14 | Metal deposition | Metal deposition | Metal deposition |
| 15 | Post Metal Annealing (PMA) | Post Metal Annealing (PMA) | Post Metal Annealing (PMA) |
| 16 | Metal etching | Metal etching | Metal etching |

*Appendix 3.1*: short process flow of the three doping alternatives.

ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

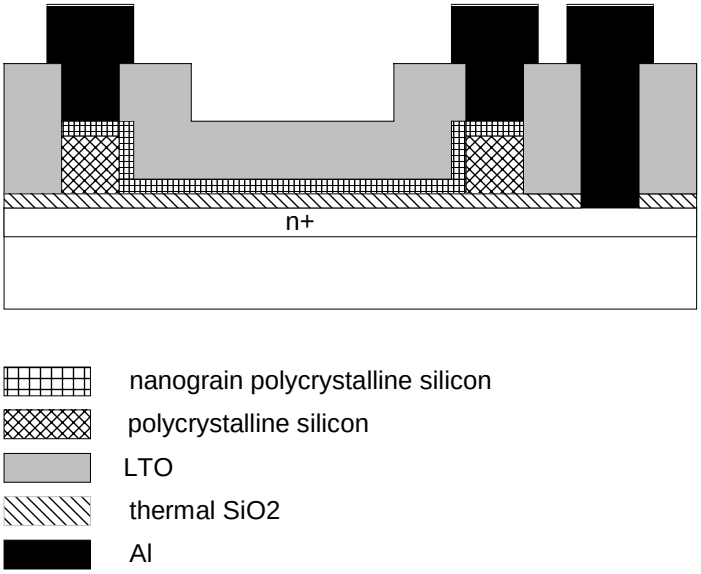
# MEMOWIRE

## General Planning of Activities

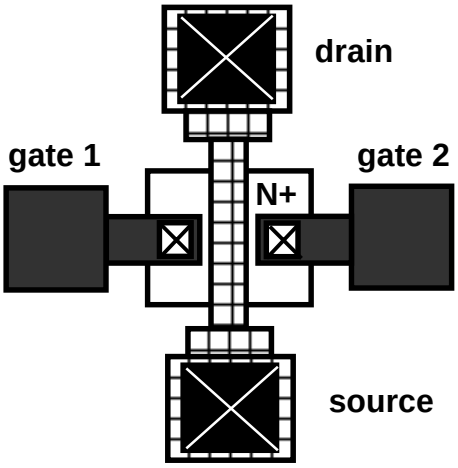
Project duration: 9 months
Project start/end date: 15 November 2001 / 15 July 2002

## Type of Activities:

1) **Process flow setup** - Duration: 1 month (Nov. 15th – Dec.15th 2001).
   MEMOWIRE's process flow defined by EPFL is given in **Appendix 1**.
   The process flow includes the use of an optimized LPCVD deposition process for the nano-grain ultra-thin polysilicon films. A detailed initial study of various deposition techniques for ultra-thin polysilicon films has been performed preceding the start date of this project (see publication given **Appendix 2**), as a step in the EPFL's Few-Electron Electronics internal project. The selected deposition technique is based on the LPCVD deposition of a 6-nm amorphous ultra-thin silicon layer (at 500°C, 300mTorr) on top of a 7nm-thick thermal oxide, followed by recrystallization (at 700°C, 10min). A simplified schematic of one typical original proposed device is given in Fig. 1.
2) **Optimization of the implant parameters via 1-D numerical simulation (TCAD)** – Duration: 2 months (Dec. 15th 2001 – February 15th 2002).
   Various combinations of the implantation parameters: (I) *implant energy*, (II) *dose* and (III) *nature of the dopant* (at least P, B and As will be considered) will be investigated using Silvaco's Athena software. The simulation concerns polycrystalline silicon films with thickness less than 20nm on top of a 5 to 10 nm thick thermal oxide layer. Complementary predictions will concern the expected resistivity of the implanted ultra-thin films; however, the resistivity estimation is not expected to be very accurate since Athena is not able to take into account the grain size influence, which is a key factor for the conductivity of the polycrystalline silicon. It is worth noting that, according to the process flow defined at 1), all the necessary process steps prior to implantation will be carried out in parallel, including the design of masks.
3) **Ion Implantation** – Duration: 3 months (February 15th 2002 - May 15th 2002). The estimated number of wafers to be implanted is 75. The estimated number of runs is 3 to 5. Various splits will be defined according to results obtained at 2) in the frame of a DOE (Design-Of-Experiment). Close collaboration with Dr. J. Tringe is projected to define the final DOE. The company which will perform the implantation is one of the two following candidates: (1) **Colybris,** Neuchâtel, Switzerland, and (2) **Ion Beam Services**, Marseille, France. Contacts have been established and the selection will be based on their final offer.
4) **Electrical and physical characterization** – Duration: 4 months (March 15th 2002 – July 15th 2002).
   The electrical (I-V, C-V) and physical characterization (SEM, TEM, AFM) of the fabricated structures will be carried out by the Swiss Federal Institute of Technology Lausanne (EPFL). A test device will be provided to Dr. J. Tringe for electrical characterization.




(a)




(b)

Fig. 1 a) Cross section of one typical ‘MEMOWIRE’ device, b) top view of the same device.

# NOVEL TECHNIQUE FOR NANOGRAIN ULTRA-THIN POLYSILICON FILM DEPOSITION AND IMPLANTATION†

S. Ecoffey, D. Bouvet, P. Fazan, J. W. Tringe*, A. M. Ionescu

Swiss Federal Institute of Technology, Electronic Laboratories, CH-1015 Lausanne, Switzerland
*U.S. Air Force Research Laboratory, Space Vehicles Directorate, USA

*Abstract*–**A new process for the fabrication of nanograin ultra-thin phosphorous-doped polysilicon film is presented. The process involves a two-step polysilicon Low Pressure Chemical Vapour Deposition (LPCVD) and a low energy "hot" implantation process at 500°C. With these techniques, we have carried out the deposition of layers of less than 10nm, which have shown resistivities around 1.cm. Systematic measurements carried out with 4-point probe configuration have been used to investigate the conduction in those films. We have observed charge trapping that induces hysteresis in the I-V characteristics.**

## 1. INTRODUCTION

The present minimum feature size (130–180nm) in integrated circuits will be decreased below 100nm (around 30–50nm) by 2014. According to the SIA's National Roadmap for Semiconductors, by 2014, current CMOS devices and circuits will reach their physical and functional limitations because of quantum effects, currently neglected in carrier transport. This device dimension region is described as a "no known solution/high risk"domain .

Recently, Single Electron Devices (SEDs) have come to be considered as promising future candidates for future ultra-low power, high-density integrated circuits. A Single Electron Memory (SEM) exploits the trapping or detrapping of a single electron to a conductive island that modifies its potential. Different classes of SEM have been reported: (i) single island SEM [1], (ii) multi islands SEM [2], nanocrystals SEM [3]. An alternative for those memories is an ultra-thin polysilicon wire in which each grain represents an island [4]; the critical technological steps for this type of SEM lie in the deposition and the ion implantation of an ultra-thin polysilicon film with nanometer-size grains.

This paper presents a novel method for the completion of an ultra-thin phosphorous ion implanted polysilicon film. The process involves a two-step LPCVD polysilicon deposition and a low energy "hot" implantation at 500°C.

0-7803-7821-0/03/$17.00 

## 2. ULTRA-THIN FILM DEPOSITION

The deposition of the ultra-thin (<10nm) polysilicon film has been carried out in a standard horizontal hot wall LPCVD reactor using pure silane as reactant gas. The substrates used were 100mm ‹100› oriented, boron-doped p-type silicon wafers with a 500Å thermal oxide grown on the surface.

A two-step process with an amorphous silicon (a Si) deposition followed by a thermal crystallization anneal has been used [5]. This method allows the formation of 6nm polysilicon thick films with grain sizes ranging from 10 to 20nm (see Fig. 1).

The a–Si deposition has been achieved at 500°C under a silane pressure of 300mTorr, whereas the crystallization has been carried at 700°C during 10min.

**Fig. 1.** Dark field TEM image of a 10nm polysilicon film annealed ten minutes at 700 °C; the white area represents a grain.

## 3. ULTRA-THIN FILM IMPLANTATION

The need to keep the polysilicon grain sizes acceptable (around 10nm) has prevented the use of a standard implantation process

followed by high temperature anneal. The high temperature activation anneal would have led to unacceptable grain growth. Hence, a novel method of implantation is proposed here: a "hot" implantation at 500°C where a part of the dopants are already activated during implantation. This method allows lowertemperature activation anneals following implantation, or even avoidance of the anneal altogether in some cases..

The thickness of the polysilicon film to be implanted (10nm) and the use of this novel process have made mandatory an ion implantation simulation based study. For this purpose, ATHENA, a 2D process simulation software from Silvaco International has been exploited. Two models have been used for this study: a SIMS Verified Dual Pearson (SDVP) model, and a Monte Carlo (MC) model for the "hot" implantation at 500°C. The simulation has been focused on the implantation with low energies (5 to 25keV), in order to prevent the degradation of the polysilicon ultra-thin film and the underlying "gate" oxide. Phosphorous has been chosen as doping species.

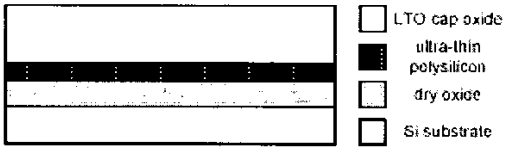



**Fig. 2.** Cross section of the structure exploited for the ion implantation based study.

The basic structure used for the simulation is represented on Fig. 2. It consists of a Low Temperature Oxide (LTO) cap layer deposited on the 10nm ultra-thin polysilicon film and a 50nm dry oxide. The cap oxide acts as an ultrathin film protection and is essential for the calibration of the appropriate energy and dose of implantation for a given impurity concentration in the film.

Figure 3 shows the SVDP simulated doping profile of an ultra-thin polysilicon layer implanted at three different energies: 22, 24 and 26keV, and annealed at 700°C for 10min. We can see that, for a given cap oxide thickness (80nm), a small variation of the implantation energy causes drastic changes of the doping profile. At 22keV the ultra-thin film is very lightly doped, whereas at 26keV it is doped around $5x10^{19}cm^{-3}$ and the underlying dry oxide is weakened by the presence of phosphorous impurity. The 24keV being the appropriate energy for an 80nm cap oxide layer.

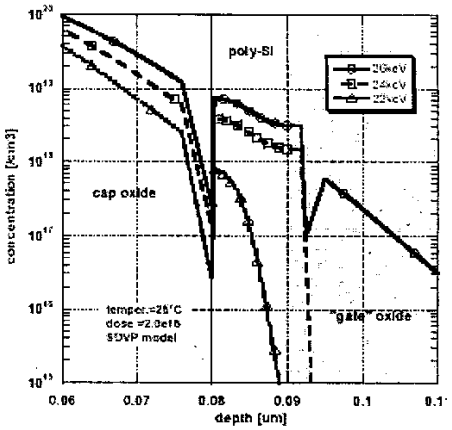



**Fig. 3.** SVDP simulated doping profile of a phosphorous ion implanted polysilicon film.

This energy sensitivity is due to the minimal thickness (about 10nm) of the layers involved in this process. Therefore, the cap oxide has become an essential parameter for calibration of the doping profile in the polysilicon film.

The effect of temperature on ion implantation has also been evaluated. Fig. 4 presents the MC simulated doping profile of a 15keV phosphorous implanted layer. The cap oxide layer is 42nm thick. We can see that even at high temperature (800°C) the concentration in the thin film ($5.6x10^{19}cm^{-3}$) is only 10% higher than an implantation at room temperature ($5.1x10^{19}cm^{-3}$). The lowest concentration is given by an implantation at 700°C ($4.7x10^{19}cm^{-3}$), which contradicts the monotonically doping increase with temperature suggested by all the other curves. Further simulations are in progress to investigate the validity of this particular result (in fact, not used in the practical implantation). The temperatures involved for the "hot" implantation process explain the small modifications observed in the phosphorous concentration. In fact, these temperatures are too low for an increase of the impurity due to diffusion, especially for this poly-Si thickness and range of implantation energies. Diffusion

effects would be more dominant at 1000°C or more.

Finally, the 500°C implantation process was chosen in order to avoid the crystallization of the film that occurs above 550°C. The implant parameters# are the following: temperature: 500°C, energy: 15keV, and dose: $2x10^{15}cm^{-2}$. The final concentration in the polysilicon film after a 10min anneal at 700°C is around $3x10^{19}cm^{-3}$.

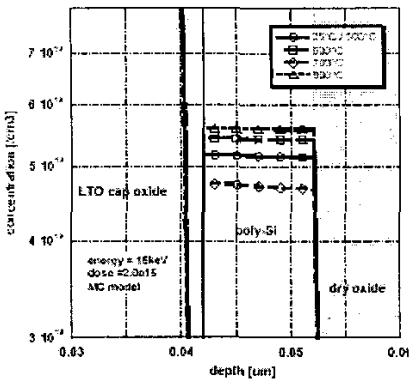



**Fig. 4.** MC simulated doping profile of a phosphorous "hot" ion implanted polysilicon film.

## 4. TEST STRUCTURE FABRICATION

In order to evaluate the resistivity of the ultra-thin polysilicon film different types of structures with varying geometries and dimensions have been designed: Van der Pauw(VdP) structures (circles, squares and crosses), 4-contact lines, and 4-contact serpentines.

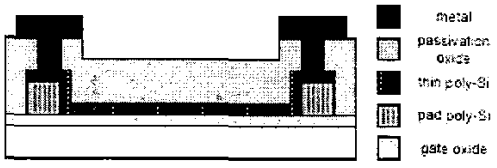



**Fig. 5.** Cross-section view of a VdP structure.

Figure 5 presents a cross-section of a VdP structure measured. One can see that polysilicon pads have been deposited in the contact region to prevent metal diffusion through the 10nm ultra-thin film and the underlying 50nm thermal "gate" oxide. Those 100nm polysilicon pads have been LPCVD deposited at 640°C and $POCl_3$ doped at 880°C. 500nm LTO has been deposited for the passivation and 800nm AlSi 1% has been used the contacting of the ultra-thin film.

## 5. RESISTIVITY MEASUREMENTS

All the electrical measurements have been carried out with a HP 4156C analyser from Agilent Technologies.

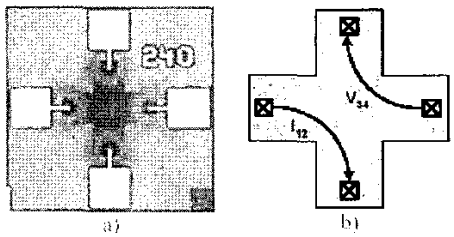



**Fig. 6.** Top views of a 240x100µm cross VdP structure: a) optical microscope picture; b) schematic.

For the VdP structures, the resistance is calculated by dividing the current forced between two probes by the voltage measured between the two others (see Fig. 6 b). The measure is repeated with a current forced between two other adjacent contacts and, by averaging the results, one can calculate the sheet resistance $R_s$ [6]:

$$Rs = 4.532R = 4.532\frac{1}{2}\left(\frac{V_{34}}{I_{12}}+\frac{V_{14}}{I_{23}}\right) \quad (1)$$

where $R$ is the average resistance and $I$ and $V$ the measured currents and voltages. The resistivity, $\rho$, is obtained by multiplying the sheet resistance, Rs, by the thickness $t$ of the film:

$$\rho = R_s t \quad (2)$$

For the wires, the resistance $R$ is simply given by dividing the voltage measured between the two internal probes by the current forced between the two external probes (see Fg. 7). The resisitivity is then calculated:

$$P = R\frac{l}{wt} = \frac{V_{23}}{I_{14}}\frac{l}{wt} \quad (3)$$

where $l$ is the length between the internal probes, $w$ and $t$ the width and thickness of the wire respectively.

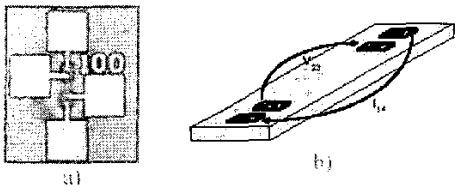


**Fig. 7.** Top view of a 100x10μm wire structure: a) optical microscope picture and b) schematic.

Table 1 reports the results of the resistivity measurements obtained on the different structures: the resistivity of our phosphorousdoped ($3x10^{19}cm^{-3}$) ultra-thin (10nm) films is around 1..cm, with a maximum estimation given by the 4–contact wires (1.28Ωcm) and a minimum value by the VdP crosses (0.72 Ωcm).

**Table 1**. Measured resistance and calculated resistivity on different structures (values averaged on 10 devices of ach type).

| Structures | $R$ [Ohm] | $\rho$ [Ohm.cm] |
|---|---|---|
| 4-contacts wires | $6.42x10^{6}$ | 1.28 |
| Serpentine (5 arms) | $5.81x10^{7}$ | 1.16 |
| Serpentine (11 arms) | $1.31x10^{8}$ | 1.12 |
| VdP (crosses) | $1.6x10^{5}$ | 0.72 |
| VdP (circles) | $1.68x10^{5}$ | 0.76 |
| VdP (squares) | $1.69x10^{5}$ | 0.77 |

The resistivity of a "thick" polysilicon film with a phosphorous concentration of $10^{19}cm^{-3}$ is around 0.01Ωcm whereas at $10^{18}cm^{-3}$ it increases to 1Ωcm, [7]. Considering that with the "hot" implantation process, only 50 to 60% of the dopants are activated and that the reduction of the film thickness increases the resistivity [8], the measurements are in good agreement with final simulated phosphorous concentration of $3x10^{19}cm^{-3}$.

Figure 8 presents a typical I-V curve obtained on a LxW=100x10μm ultra-thin polysilicon wire placed on a 50nm-thick oxide. The substrate is biased as the gate of pseudotransistor and the two contacts of the wires are biased as the 'source' and 'drain'. All the measured polysilicon wires have shown a reproducible hysteresis of the I-V characteristics, which demonstrates the presence of charge trapping in the ultra-thin film or at the polysilicon/oxide interface. This is supported by the observation that this effect is enhanced when the gate voltage is increased towards higher values (compare 3V, 10V, 15V and 20V curves in Fig. 8). Further measurements of the time responses of the trapping process are in progress in order to distinguish the dominant charge trapping mechanism and correlate it with the dooping level. It is worth noting that this hysteresis effect suggest the exploitation of such small polysilicon wires as elementary memory elements ('*memowires*').

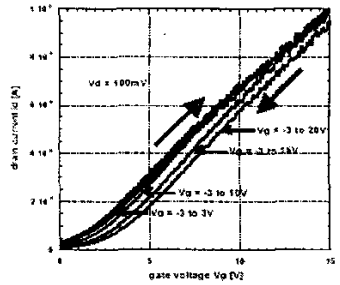


**Fig. 8.** a) I-V characteristics of a 100x10μm ultra-thin polysilicon wire.

## 6. CONCLUSION

A two-step fabrication technique for ultrathin (<10nm) nano-grain polysilicon films was proposed: (i) deposition of less-than-10nm amorphous silicon (aSi) followed by a thermal crystallization anneal, and, (ii) implantation of the 10nm polysilicon films without the need of a high thermal budget for dopant activation, using a hot wafer (500°C) process.

The resistivity of a phosphorous "hot" implanted polysilicon film ($3x10^{19}cm^{-3}$) is about 1Ωcm, and all the elementary devices made on such films have shown significant hysteresis effect at room temperature, which make them potential candidates for future Single Electron Memory.

**Acknowledgments:** †This project has been funded by the European Office of Aerospace Research and Development (EOARD), London, UK, Research contract: F61775-02-WD079-MEMOWIRE.

# The ion implantation was been performed by Ion Beam Services (IBS) in Peynier, France.

### References

[1] S. Chou et al, *App. Phys. Letts.*, **70** (7), pp. 850–852, 1997.
[2] A. Dutta et al, *App. Phys. Letts.*, **75** (10), pp. 14422–1424, 1999.
[3] J.De Blauwe, *IEDM'00*, pp. 683–686, 2000.
[4] K. Yano et al, *IEEE Transactions on Electron Devices*, **41** (9), pp. 1628–1638, 1994.
[5] S. Ecoffey et al, *Nanotechnology*, **13** (3), pp.290–293, 2002.
[6] Y. Sun et al, *Semicond. Sci. Technol.*, **11**, pp. 805–811, 1996.
[7] M.M. Mandurah et al, *J. Electrochem. Soc.*, **126** (6), pp. 1019–1023, 1979.
[8] T. Kamins, *Polycristalline silicon for integrated circuit applications*, Kluwer, Boston, 1988.

# PROCESS FLOW: NANOWIRE TEST STRUCTURES

| Module: **Wafer start (marques ASM & Ebeam)** | | | | | | |
|---|---|---|---|---|---|---|
| | Recipe n° | Who | Tool / Localization | Measure: Tool / Localization | Measure: Recipe / Specification | Results on monitor or product |
| 1 | SPIN RESIST | LETI | - | - | - | - |
| 2 | EXPOSE RESIST | LETI | - | - | - | - |
| 3 | DEVELOP RESIST | LETI | - | - | - | - |
| 4 | Si ETCH | LETI | - | - | - | - |
| 5 | STRIP RESIST | LETI | - | - | - | - |
| 6 | SPIN RESIST | LETI | - | - | - | - |
| 7 | EXPOSE RESIST | LETI | - | - | - | - |
| 8 | DEVELOP RESIST | LETI | - | - | - | - |
| 9 | Si ETCH | LETI | - | - | - | - |
| 10 | STRIP RESIST | LETI | - | - | - | - |
| | | | | | | |
| COMMENTS: | | | | | | |

| Module: **Compensation layer (0.5µm)** | | | | | | |
|---|---|---|---|---|---|---|
| | Recipe n° | Who | Tool / Localization | Measure: Tool / Localization | Measure: Recipe / Specification | Results on monitor or product |
| 11 | CLEAN | LETI | - | - | - | - |
| 12 | SACRIFICIAL OXIDE | LETI | - | - | - | - |
| 13 | SPIN RESIST | LETI | - | - | - | - |
| 14 | EXPOSE RESIST | LETI | - | - | - | - |
| 15 | DEVELOP RESIST | LETI | - | - | - | - |
| 16 | IMPLANTATION | LETI | - | - | - | - |
| 17 | STRIP RESIST | LETI | - | - | - | - |
| 18 | ACTIVATION | LETI | - | - | - | - |
| 19 | $SiO_2$ ETCH | LETI | - | - | - | - |
| | | | | | | |
| COMMENTS: | | | | | | |

| Module: **Tunnel oxide (5 – 10nm)** | | | | | | |
|---|---|---|---|---|---|---|
| Recipe n° | | Who | Tool / Localization | Measure: Tool / Localization | Measure: Recipe / Specification | Results on monitor or product |
| 20 | RCA CLEAN | EPFL | WET BENCH RCA / ZONE 3 | - | - | - |
| 21 | DRY OXIDATION | EPFL | CENTROTHERM / ZONE 3 (2_3) | ELLIPSOMETRE / ZONE 3 | OXIDE ON Si | E N C S O |
| | | | | | | |
| COMMENTS: | | | | | | |

| Module: **Contact plots (0.1 – 0.2µm)** | | | | | | |
|---|---|---|---|---|---|---|
| Recipe n° | | Who | Tool / Localization | Measure: Tool / Localization | Measure: Recipe / Specification | Results on monitor or product |
| 22 | LPCVD POLY-Si | EPFL | CENTROTHERM / ZONE 3 (1_1) | NAOSPEC 6100 / ZONE 3 | POLY ON $SiO_2$ / Si | E N C S O |
| 23 | $POCl_3$ DOPING | EPFL | CENTROTHERM / ZONE 3 (1_4) | 4 P. MEASURE / ZONE 4 | POLY 13 pts | M1 M2 M3 P1 P2 P3 |
| 24 | DEGLAZE | EPFL | ZONE 2 | - | - | - |
| 25 | SPIN RESIN | EPFL | RITE TRACK (Track 1) / ZONE 1 | - | - | - |
| 26 | EXPOSE RESIST | EPFL | ZONE 1 | - | - | - |
| 27 | DEVELOP RESIST | EPFL | RITE TRACK (Track 2) / ZONE 1 | - | - | - |
| 28 | POLY-Si ETCH | EPFL | DRY OR WET / ZONE 2 | MICROSCOPIC INSPECTION / ZONE 3 | - | - |
| 29 | STRIP RESIST WET | EPFL | WET BENCH PHOTO / ZONE 3 | - | - | - |
| 30 | STRIP RESIST PLASMA | EPFL | TEPLA / ZONE 5 OXFORD / ZONE 2 | MICROSCOPIC INSPECTION / ZONE 3 | - | - |
| | | | | | | |
| COMMENTS: | | | | | | |

| Module: **Nanograin thin film deposition (10nm)** | | | | | | |
|---|---|---|---|---|---|---|
| Recipe n° | | Who | Tool / Localization | Measure: Tool / Localization | Measure: Recipe / Specification | Results on monitor or product |
| 31 | DIP HF | EPFL | CENTROTHERM / ZONE 3 (1_4) | 4 P. MEASURE / ZONE 4 | POLY 13 pts | M1 M2 M3 P1 P2 P3 |
| 32 | LPCVD a-Si | EPFL | CENTROTHERM / ZONE 3 (1_1) | ELLIPSOMETRE / ZONE 3 | a-Si ON $SiO_2$ / Si | E N C S O |
| 33 | ANNEALING | EPFL | CENTROTHERM / ZONE 3 (2_1) | TEM / CIME EPFL | - | PICT : |
| 34 | SACRIFICIAL OXIDE | EPFL | CENTROTHERM / ZONE 3 (2_2) | - | - | - |
| 35 | SPIN RESIST | EPFL | RITE TRACK (Track 1) / ZONE 1 | - | - | - |
| 36 | EXPOSE RESIST | EPFL | ZONE 1 | - | - | - |
| 37 | DEVELOP RESIST | EPFL | RITE TRACK (Track 2) / ZONE 1 | - | - | - |
| 38 | IMPLANTATION | - | - | - | - | - |
| 39 | ACTIVATION | - | - | - | - | - |
| 40 | STRIP RESIST WET | EPFL | WET BENCH PHOTO / ZONE 3 | - | - | - |
| 41 | STRIP RESIST DRY | EPFL | TEPLA / ZONE 5 OXFORD / ZONE 2 | MICROSCOPIC INSPECTION / ZONE 3 | - | - |
| 42 | $SiO_2$ ETCH | EPFL | DRY OR WET / ZONE 2 | MICROSCOPIC INSPECTION / ZONE 3 | - | - |
| | | | | | | |
| COMMENTS: | | | | | | |

| Module: **Nanograin thin film implantation** | | | | | | |
|---|---|---|---|---|---|---|
| Recipe n° | | Who | Tool / Localization | Measure: Tool / Localization | Measure: Recipe / Specification | Results on monitor or product |
| 43 | CLEAN | EPFL | WET BENCH RCA / ZONE 3 | - | - | - |
| 44 | SACRIFICIAL OXIDE | EPFL | CENTROTHERM / ZONE 3 (2_2) | - | - | - |
| 45 | SPIN RESIST | EPFL | RITE TRACK (Track 1) / ZONE 1 | - | - | - |
| 46 | EXPOSE RESIST | EPFL | ZONE 1 | - | - | - |
| 47 | DEVELOP RESIST | EPFL | RITE TRACK (Track 2) / ZONE 1 | - | - | - |
| 48 | **IMPLANTATION N** | **Subcontr**. | - | - | - | - |
| 49 | STRIP RESIST WET | EPFL | WET BENCH PHOTO / ZONE 3 | - | - | - |
| 50 | STRIP RESIST DRY | EPFL | TEPLA / ZONE 5 OXFORD / ZONE 2 | MICROSCOPIC INSPECTION / ZONE 3 | - | - |
| 51 | SPIN RESIST | EPFL | - | - | - | - |
| 52 | EXPOSE RESIST | EPFL | ZONE 1 | - | - | - |
| 53 | DEVELOP RESIST | EPFL | RITE TRACK (Track 2) / ZONE 1 | - | - | - |
| 54 | **IMPLANTATION P** | **Subcontr.** | - | - | - | - |
| 55 | STRIP RESIST WET | EPFL | WET BENCH PHOTO / ZONE 3 | - | - | - |
| 56 | STRIP RESIST DRY | EPFL | TEPLA / ZONE 5 OXFORD / ZONE 2 | MICROSCOPIC INSPECTION / ZONE 3 | - | - |
| 57 | SPIN RESIST | EPFL | - | - | - | - |
| 58 | EXPOSE RESIST | EPFL | ZONE 1 | - | - | - |
| 59 | DEVELOP RESIST | EPFL | RITE TRACK (Track 2) / ZONE 1 | - | - | - |
| **60** | **IMPLANTATION N+** | - | - | - | - | - |
| 61 | STRIP RESIST WET | EPFL | WET BENCH PHOTO / ZONE 3 | - | - | - |
| 62 | STRIP RESIST DRY | EPFL | TEPLA / ZONE 5 OXFORD / ZONE 2 | MICROSCOPIC INSPECTION / ZONE 3 | - | - |
| 63 | SPIN RESIST | EPFL | - | - | - | - |
| 64 | EXPOSE RESIST | EPFL | ZONE 1 | - | - | - |
| 65 | DEVELOP | EPFL | RITE TRACK (Track 2) / | - | - | - |

| | | | | | | |
|---|---|---|---|---|---|---|
| | RESIST | | ZONE 1 | | | |
| **66** | **IMPLANTATION P+** | **Subcontr.** | - | - | - | - |
| 67 | STRIP RESIST WET | EPFL | WET BENCH PHOTO / ZONE 3 | - | - | - |
| 68 | STRIP RESIST DRY | EPFL | TEPLA / ZONE 5 OXFORD / ZONE 2 | MICROSCOPIC INSPECTION / ZONE 3 | - | - |
| 69 | SPIN RESIST | EPFL | - | - | - | - |
| 70 | EXPOSE RESIST | EPFL | ZONE 1 | - | - | - |
| 71 | DEVELOP RESIST | EPFL | RITE TRACK (Track 2) / ZONE 1 | - | - | - |
| **72** | **IMPLANTATION N++** | **Subcontr.** | - | - | - | - |
| 73 | STRIP RESIST WET | EPFL | WET BENCH PHOTO / ZONE 3 | - | - | - |
| 74 | STRIP RESIST DRY | EPFL | TEPLA / ZONE 5 OXFORD / ZONE 2 | MICROSCOPIC INSPECTION / ZONE 3 | - | - |
| 75 | $SiO_2$ ETCH | EPFL | DRY OR WET / ZONE 2 | MICROSCOPIC INSPECTION / ZONE 3 | - | - |
| | | | | | | |
| COMMENTS: | | | | | | |

Module: **Nanograin thin film lithography**

| Recipe n° | | Who | Tool / Localization | Measure: Tool / Localization | Measure: Recipe / Specification | Results on monitor or product |
|---|---|---|---|---|---|---|
| 76 | CLEAN | LETI | - | - | - | - |
| 77 | SPIN RESIST | LETI | - | - | - | - |
| 78 | EXPOSE RESIST | LETI | - | - | - | - |
| 79 | DEVELOP RESIST | LETI | - | - | - | - |
| 80 | FILM ETCH | LETI | - | - | - | - |
| 81 | STRIP RESIST | LETI | - | - | - | - |
| | | | | | | |
| COMMENTS: | | | | | | |

| Module: **Passive oxide deposition (0.3µm)** | | | | | | |
|---|---|---|---|---|---|---|
| Recipe n° | | Who | Tool / Localization | Measure: Tool / Localization | Measure: Recipe / Specification | Results on monitor or product |
| 82 | RCA CLEAN (NO HF) | EPFL | WET BENCH RCA / ZONE 3 | - | - | - |
| 83 | LTO OXIDE | EPFL | LTO (ALCATEL) / ZONE 3 | NANOSPEC 6100 / ZONE 3 | OXIDE | E N C S O |
| 84 | SPIN RESIST | EPFL | RITE TRACK (Track 1) / ZONE 1 | - | - | - |
| 85 | EXPOSE RESIST | EPFL | ZONE 1 | - | - | - |
| 86 | DEVELOP RESIST | EPFL | RITE TRACK (Track 2) / ZONE 1 | - | - | - |
| 87 | $SiO_2$ ETCH | EPFL | DRY OR WET / ZONE 2 | MICROSCOPIC INSPECTION / ZONE 3 | - | - |
| 88 | STRIP RESIST WET | EPFL | WET BENCH PHOTO / ZONE 3 | | - | |
| 89 | STRIP RESIST PLASMA | EPFL | TEPLA / ZONE 5 OXFORD / ZONE 2 | LEO1550 / ZONE 1 | - | PICT: |
| | | | | | | |
| COMMENTS: | | | | | | |

| Module: **Metallization** | | | | | | |
|---|---|---|---|---|---|---|
| Recipe n° | | Who | Tool / Localization | Measure: Tool / Localization | Measure: Recipe / Specification | Results on monitor or product |
| 90 | PVD Ti/N | EPFL | BAS450 / ZONE 4 | 4 P. MEASURE / ZONE 4 | Metal 13 pts | M1 P1<br>M2 P2<br>M3 P3 |
| 91 | PVD Ti | EPFL | BAS450 / ZONE 4 | 4 P. MEASURE / ZONE 4 | Metal 13 pts | M1 P1<br>M2 P2<br>M3 P3 |
| 92 | PVD AlSi | EPFL | BAS450 / ZONE 4 | 4 P. MEASURE / ZONE 4 | Metal 13 pts | M1 P1<br>M2 P2<br>M3 P3 |
| 93 | SPIN RESIST | EPFL | RITE TRACK (Track 1) / ZONE 1 | - | - | - |
| 94 | EXPOSE RESIST | EPFL | ZONE 1 | - | - | - |

| | | | | | | |
|---|---|---|---|---|---|---|
| 95 | DEVELOP RESIST | EPFL | RITE TRACK (Track 2) / ZONE 1 | - | - | - |
| 96 | METAL ETCH | EPFL | DRY OR WET / ZONE 2 | MICROSCOPIC INSPECTION / ZONE 3 | - | - |
| 97 | STRIP RESIST WET | EPFL | WET BENCH PHOTO / ZONE 3 | | - | |
| 98 | STRIP RESIST PLASMA | EPFL | TEPLA / ZONE 5 OXFORD / ZONE 2 | LEO1550 / ZONE 1 | - | PICT: |
| | | | | | | |
| COMMENTS: | | | | | | |

# LPCVD deposition techniques for nanograin sub-10nm polysilicon ultra-thin films

Serge Ecoffey, Didier Bouvet, Adrian M. Ionescu and Pierre Fazan
Swiss Federal Institute of Technology, Electronic Laboratories, CH-1015 Lausanne, Switzerland

## ABSTRACT

This paper investigates the limits of a low pressure chemical vapour deposition (LPCVD) technique for the deposition of a nanometer scale ultra-thin polysilicon (poly-Si) film with sub-10nm grain sizes. Three different processes using pure silane ($SiH_4$) in a standard horizontal hot-wall reactor are presented: (i) a direct poly-Si deposition, (ii) a Hemispherical Silicon Grain (HSG) deposition and (iii) an amorphous silicon (a-Si) deposition followed by a thermal crystallization anneal. The direct poly-Si deposition gives a minimum film thickness achievable around 20 nm with grain sizes ranging from 20 to 30 nm. The HSG deposition process leads to the formation of grains with diameters varying from 5 to 50 nm and heights ranging from 5 to 20 nm. The best results are obtained with the third process (a-Si / crystallization), which allows the formation of 6 nm poly-Si thick films with grain sizes ranging from 10 to 20 nm.

## INTRODUCTION

According to the 1999 International Technology Roadmap for Semiconductors (ITRS) [1], it is recognized that “no known solutions” in virtually all of the technology areas will be encountered by 2008 with the shrinkage of the feature size in integrated circuits below 20 – 30 nm. Single Electron Devices (SED) are projected to be alternative components for ultra-large scale integration (ULSI). Present temperature operation of SED's is less than 20K, but room temperature operated memories have already been demonstrated [2-5]. In those devices, the transfer of a single electron is made possible thanks to the Coulomb blockade effect [6]. To be efficient at room temperature, the Coulomb blockade needs nanometer size devices that cannot be achievable with actual lithographic limitations. Therefore most of the SE memories [2-5] consist of nanometer scale separated Si islands that can store a charge of one electron per island. A recent work on a poly-Si wire in which each grain represents an island [7] let us think that an ultra-thin poly-Si wire with nanograins could be an alternative for those devices. In this case, it clearly appears that the critical technological step lies in the deposition of an ultra-thin poly-Si film with grain sizes of less than 10 nm.

This paper presents the evaluation of three different LPCVD processes to achieve the deposition of an ultra-thin nanograin poly-Si film: (i) a direct poly-Si deposition, (ii) a HSG deposition and (iii) an a-Si deposition followed by a crystallization thermal annealing.

## EXPERIMENTAL DETAILS

All the depositions were completed on 100 mm ‹100› oriented, boron-doped p-type silicon wafers with a 70 Å thick silicon dry oxide grown on the surface. The LPCVD system is a conventional horizontal hot wall reactor using pure silane as reactant gas. In the following, three different processes are reported.

The poly-Si deposition is a more common process. It is well known [8] that the crystalline structure depends on the deposition temperature and the silane pressure, and the transition region

between amorphous and crystalline phase is set around 560 and 590 °C for a silane pressure around 150 mTorr. Increasing the pressure at a given temperature increases the degree of amorphization. Hence, the direct poly-Si deposition process is characterized for temperatures ranging from 580 to 640 °C with silane pressures varying from 60 to 200 mTorr.

Sallese *et al* [9] have demonstrated that the HSG deposition process could be assumed as a two steps process in which the first step consists in a simple a-Si deposition, whereas the second is an in-situ anneal at higher temperatures leading to the formation of crystalline silicon grains by Si atom migration on the surface, as shown on figure 1. The grain diameters and heights are influenced by the annealing temperature and time, by the presence of silane during anneal, and also by the thickness of the a-Si layer. Therefore, the effect of the a-Si deposition temperature between 500 and 525 °C is analysed, while the annealing step is maintained at 545 °C. The silane pressure is kept at 150 mTorr.

The a-Si / crystallization process is also investigated as a two steps process. The first step consists in a-Si deposition at temperature below 550 °C as defined before, while the second step is a Solid Phase Crystallization (SPC) at temperatures higher than 600 °C. The difference with the HSG process is due to the formation of a native oxide on the wafer surface prior to thermal annealing. This native oxide prevents the migration of the Si atoms and so the HSG formation. The a-Si films are deposited at temperatures and silane pressure ranging from 475 to 525 °C and 150 to 350 mTorr. The SPC is carried out in the same LPCVD system, under a nitrogen atmosphere and with temperatures varying from 700 to 950 °C.

The gas flux is fixed at 30 sccm in the back of the reactor for the three processes. The thickness measurements are made by ellipsometry. The surface morphologies are observed by Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM), whereas the microstructures are investigated by Transmission Electron Microscopy (TEM).

## DISCUSSION

The LPCVD poly-Si deposition involves high deposition rates that are interesting for thick films applications. For deposition temperatures ranging from 580 to 640 °C, the slopes of the calibration curves gives deposition rates varying from 30 to 68 Å/min (see table I). Even with a silane dilution in nitrogen in a ratio of one volume silane per thirty-two volumes of nitrogen, the deposition rate cannot be decreased to less than 30 Å/min.

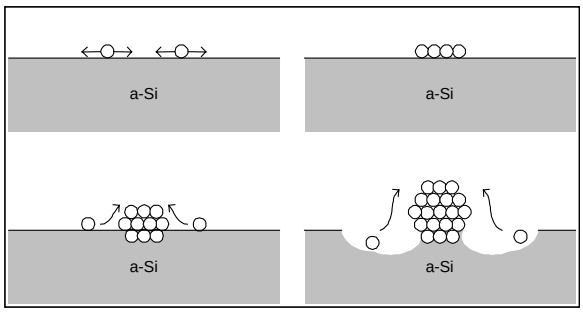


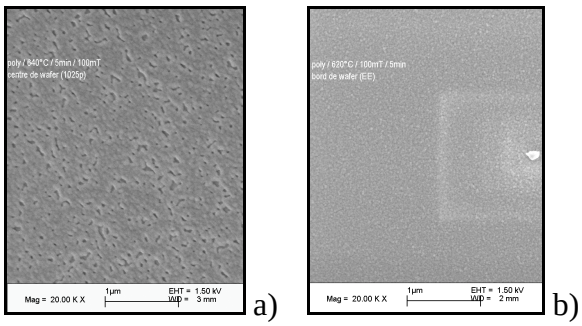

**Figure 1.** Schematic growth sequence of a Hemispherical Silicon Grain (HSG). The second step of the process (thermal anneal) is represented.

**Table I.** Deposition rate and minimum thickness to get a continuous surface vs deposition rate and silane pressure for a direct poly-Si deposition.

| Dep. temp. (°C) | Pressure (mTorr) | Dep. rate (Å $min^{-1}$) | Cont. surface at – (Å) |
|---|---|---|---|
| 640 | 100 | 68 | 330 |
| 620 | 100 | 60 | 280 |
| 600 | 100 | 36 | 200 |
| 580 | 200 | 30 | - |

Table 1 also shows that the deposition rate influences the morphology of the film. Indeed, the higher the deposition rate is, the thicker the film must be to fully recover the all surface. At 640 °C the deposition rate is about 68 Å/min and the minimum film thickness to avoid porosity stands around 330 Å, whereas at 620 °C this minimum thickness decreases to 280 Å. If we assume a linear behavior of the deposition rate and this minimum film thickness, a 100 Å film would require a 12 Å/min deposition rate. However, the deposition rate cannot be lessen under 30 Å/min, which is the deposition rate for the lowest temperature (580 °C) and for the deposition with silane diluted in nitrogen. Thus, the minimum film thickness obtained is about 200 Å, and the TEM measurements on such a film give grain sizes ranging from 20 to 30 nm. Figure 2 shows two SEM micrographs, one of a 320 Å deposit at 640 °C containing porosity and the other of a 300 Å continuous film deposited at 620 °C.

A classical HSG process consists of an a-Si deposition followed by a seeding step, that is an in-situ anneal at higher temperatures, with an addition of silane at the beginning. This seeding method proposed by Sakai *et al* [10], allows a thinner grain size distribution, but causes coalescence of the HSG's for a-Si thickness around 10 nm. Thus, a ten minutes a-Si deposition at 525 °C and a silane pressure of 150mT, followed by a twenty minutes thermal anneal at 545 °C with a silane pressure of 150 mTorr during the first fifteen minutes produces grain with sizes ranging from 50 to 500 nm or more. Simply replacing silane by nitrogen during seeding allows to decrease the grain sizes around 5 to 100 nm and so to avoid coalescence too. Figure 3 presents a SEM picture of a HSG deposition carried out at 500 °C during fifteen minutes with a silane pressure of 150 mTorr for a twenty minutes annealing step at 545 °C. It gives grain diameters ranging from 5 to 50 nm and heights varying from 10 to 20 nm. This is the smallest feature obtained with this process. The reduction in grain sizes is due to the reduction of the a-Si film (~35 Å) deposited in the first step.




a) b)

**Figure 2.** SEM micrograph of poly-Si deposited at a) 640 °C (330 Å) and b) 620 °C (300 Å).

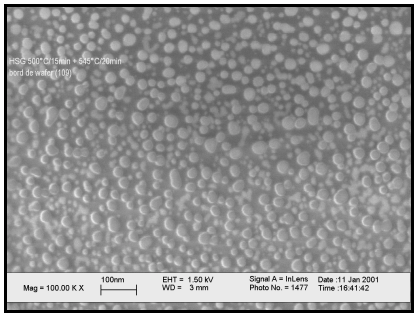


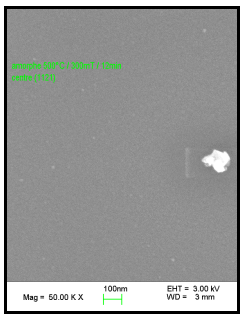

**Figure 3.** SEM micrograph of HSG. It represents a fifteen minutes a-Si deposition at 500 °C under 150 mTorr of silane, followed by a twenty minutes thermal anneal at 545 °C.

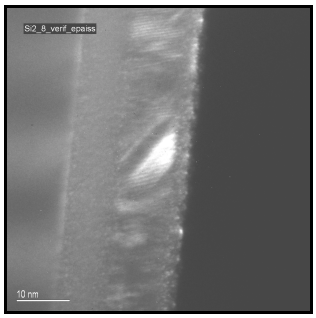
The temperatures usually exploited for thick a-Si LPCVD deposition ranges from 480 to 550 °C for silane pressure of 200 mTorr. However, the deposition of ultra-thin a-Si films is limited to temperatures around 500 °C. A deposition at 475 °C with a silane pressure of 150 mTorr presents a granular structure that increases the density and the size of the pores in a thin film (100 Å) as compared with a 500 °C layer deposited under the same conditions. Furthermore, the incubation time at 475 °C is more than sixty minutes for a deposition rate of ~3 Å/min, which is not acceptable. Depositions above 500 °C, as 525 °C for example, leads to the formation of HSG's during the reactor purge necessary to eliminate silane residue. The reactor is brought several times under vacuum conditions, what promotes, at this temperature, the silicon atom surface diffusion. The nucleation of grains is also favored by the stresses due to the thin thickness of the film.

Nevertheless, even with a deposition temperature of 500 °C and a silane pressure of 150 mTorr, the deposited films are limited to a thickness of 150 Å. For these thicknesses we encounter the same porosity problems as with the direct poly-Si deposition. Works done on the nucleation of quantum dots [11,12] have shown that there are three different ways to increase the density of nuclei at the early stage of the deposition: create OH bonds on the surface by dipping the wafer in HF prior to the deposition; replace the silicon oxide layer on the surface by silicon nitride; and finally, increase the deposition pressure. Depositions at 490 °C under a silane pressure of 150 mTorr combined with an increase in nucleation sites, due to firstly a HF dip prior to deposition and secondly the use of silicon nitride as insulator, allows to obtain continuous a-Si films with a thickness of 100 Å.

The thinnest a-Si continuous films can be achieved with the third method previously proposed, that is an increase in the silane pressure during deposition. Indeed, it permits to achieve the deposition of a continuous a-Si film as thin as 60 Å with a deposition temperature of 500 °C and a silane pressure of 300 mTorr (see figure 4).

Figure 4 shows a cross section dark field TEM image of a 100 Å film deposited at 500 °C and a silane pressure of 300 mTorr. It can be noted that a ten minutes SPC process carried out at 700 °C, causes the formation of a needle like crystalline structure with grain sizes around 10 to 20 nm; other plan view TEM pictures confirm these results. Higher annealing temperatures generate an overgrowth of the grains to sizes as large as 200 nm due to the time needed to reach such temperatures. A Rapid Thermal Annealing (RTA) tool should be the most accurate equipment to obtain smaller grains, because higher annealing temperatures allow a reduction in the grain sizes [13].



a)


b)

**Figure 4. a)** SEM micrograph of a 60 Å continuous a-Si film deposited at 500 °C under a silane pressure of 300 mTorr (the particle on the right of the image prove the quality of the focus), b) dark field TEM image of a 100 Å poly-Si film annealed ten minutes at 700 °C.

## CONCLUSION

This study shows that the poly-Si LPCVD deposition of ultra-thin films needs a control of the nucleation phase at the early stage of the deposition in order to control porosity of the films. It is demonstrated that the direct poly-Si process allows the deposition of 200 Å thick films with grain sizes ranging from 20 to 30 nm. On the other hand, HSG's with grain diameters and heights varying from 5 to 50 nm and 10 to 20 nm, respectively, can be obtained with a modification of a standard HSG process. Finally, it is demonstrated that a-Si deposition at 500 °C under a silane pressure of 300 mTorr followed by 10 min annealing at 700 °C provides films with thickness less than 10 nm and grain size between 10 to 20 nm.

## REFERENCES

1. The International Technology Roadmap for Semiconductors: Technology needs (1999 edition).
2. K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai and K. Seki, *IEEE Trans. Electron Devices* **41**, 1628 (1994).
3. S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbé and K. Chan, *Appl. Phys. Lett.* **68**, 1377 (1995).
4. A. Nakajima, T. Futatsugi, K. Kosemura, T. Fukano and N. Yokoyama, *Appl. Phys. Lett.* **70**, 1742 (1997).
5. I. Kim, S. Han, K. Han, J. Lee and H. Shin, *IEEE Electron Device Letters* **20**, 630 (1999).
6. K. Likharev, *Proceedings of the IEEE* **87**, 606 (1999).
7. C. Anghel, N. Hefyene, A. M. Ionescu, M. Declerq, J. W. Tringe and J. D. Plummer, *MRS Proceedings* **638** F12.4 (2000).
8. E. Ibok and S. Garg, *J. Electrochem. Soc.* **140**, 2927 (1993).
9. J. M. Sallese, A. Ils, D. Bouvet and P. Fazan, *J. App. Phys.* **88**, 5751 (2000).
10. A. Sakai and T. Tatsumi, *Appl. Phys. Lett.* **61**, 159 (1992).
11. T. Baron, F. Martin, P. Mur, C. Wyon and M. Dupuy, *Journal of Crystal Growth* **209**, 1004 (2000).
12. S. Miyazaki, Y. Hamamoto, E. Yoshida, M. Ikeda and M. Hirose, *Thin Solid Films* **369,** 55 (2000).
13. M. K. Hatalis and D. W. Greve, *J. App. Phys.* **63**, 2260 (1988).